

# TPS3606-33

## BATTERY-BACKUP SUPERVISOR FOR LOW-POWER PROCESSORS

SLVS335C – DECEMBER 2000 – REVISED JANUARY 2007

### features

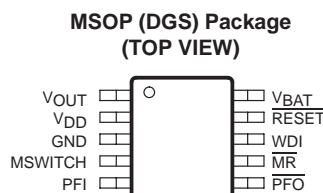
- Supply Current of 40  $\mu$ A (Max)
- Precision 3.3-V Supply Voltage Monitor  
Other Voltage Options on Request
- Watchdog Timer With 800-ms Time-Out
- Backup-Battery Voltage Can Exceed  $V_{DD}$
- Power-On Reset Generator With Fixed 100-ms Reset Delay Time
- Voltage Monitor for Power-Fail or Low-Battery Monitoring
- Manual Switchover to Battery-Backup Mode
- Manual Reset
- Battery Freshness Seal
- 10-Pin MSOP Package
- Temperature Range . . .  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

### typical applications

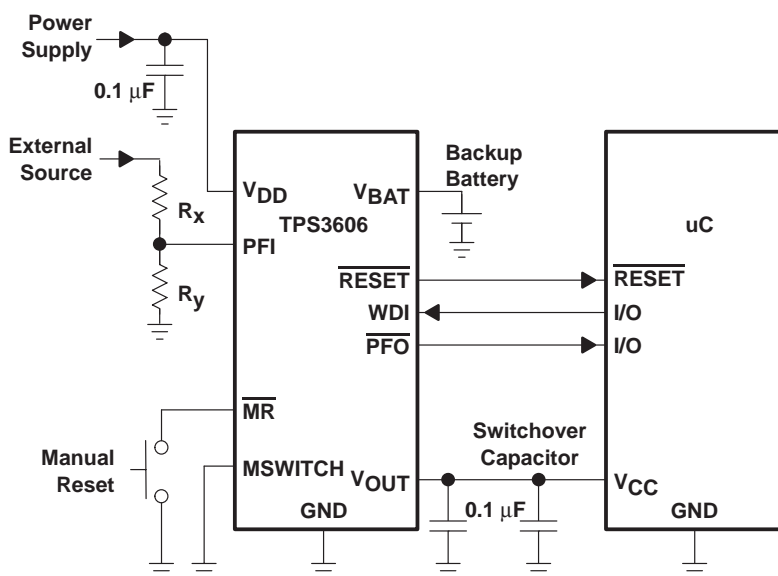
- Fax Machines
- Set-Top Boxes
- Advanced Voice Mail Systems
- Portable Battery Powered Equipment
- Computer Equipment
- Advanced Modems
- Automotive Systems
- Portable Long-Time Monitoring Equipment
- Point-of-Sale Equipment

### description

The TPS3606-33 supervisory circuit monitors and controls the processor activity. In case of power-fail or brownout conditions, the backup-battery switchover function of the TPS3606-33 allows a low-power processor and its peripherals to run from the installed backup battery without asserting a reset beforehand.



### typical operating circuit



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## description (continued)

During power on,  $\overline{\text{RESET}}$  is asserted when the supply voltage ( $V_{\text{DD}}$  or  $V_{\text{BAT}}$ ) becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors  $V_{\text{OUT}}$  and keeps the  $\overline{\text{RESET}}$  output active as long as  $V_{\text{OUT}}$  remains below the threshold voltage ( $V_{\text{IT}}$ ). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after  $V_{\text{OUT}}$  has risen above  $V_{\text{IT}}$ . When the supply voltage drops below  $V_{\text{IT}}$ , the output becomes active (low) again.

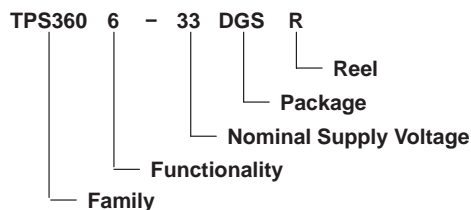
The TPS3606-33 is available in a 10-pin MSOP package and is characterized for operation over a temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

### PACKAGE INFORMATION

TA	DEVICE NAME	MARKING
$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	TPS3606-33DGSR†	AKE

† The DGSR passive indicates tape and reel of 2500 parts.

## ordering information application specific versions (see Note)



DEVICE NAME	NOMINAL VOLTAGE‡, $V_{\text{NOM}}$
TPS3606-33 DGS	3.3 V

‡ For other threshold voltages, contact the local TI sales office for availability and lead-time.

### FUNCTION TABLES TPS3606

$V_{\text{DD}} > V_{\text{SW}}$	$V_{\text{OUT}} > V_{\text{IT}}$	$V_{\text{DD}} > V_{\text{BAT}}$	$V_{\text{OUT}}$	$\overline{\text{RESET}}$
0	0	0	$V_{\text{BAT}}$	0
0	0	1	$V_{\text{DD}}$	0
0	1	0	$V_{\text{BAT}}$	1
0	1	1	$V_{\text{DD}}$	1
1	1	0	$V_{\text{DD}}$	1
1	1	1	$V_{\text{DD}}$	1

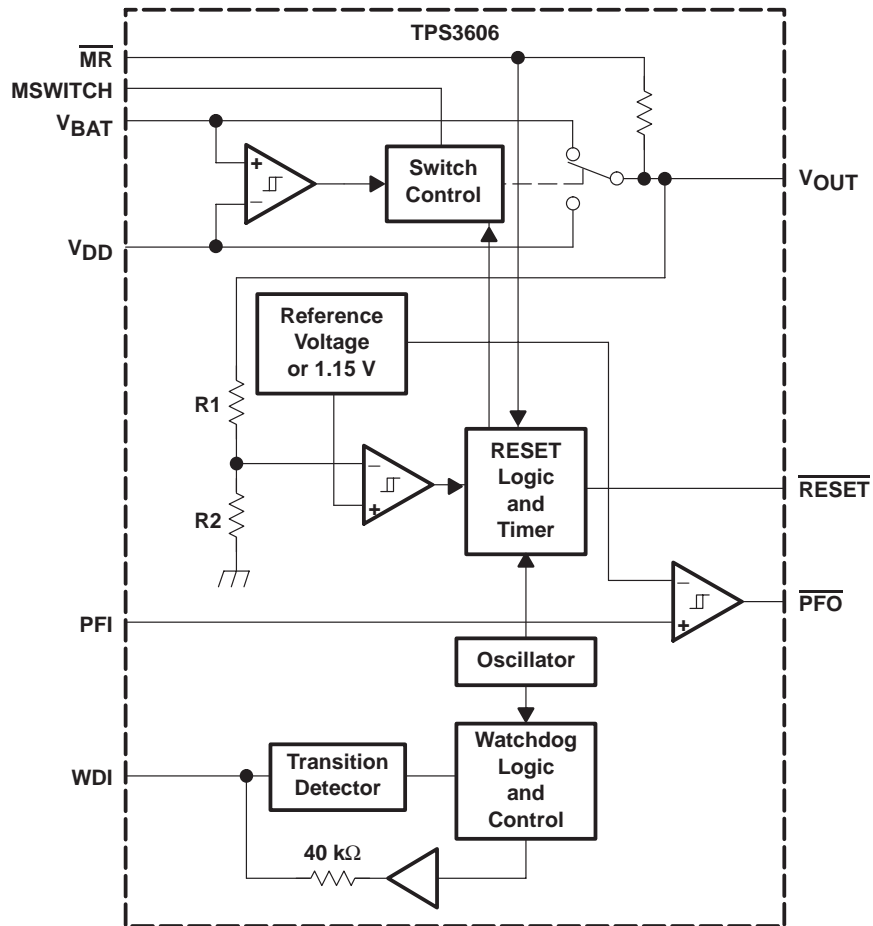
$\text{PFI} > V_{\text{PFI}}$	$\overline{\text{PFO}}$
0	0
1	1

CONDITION.:  $V_{\text{OUT}} > V_{\text{DD}}(\text{min})$

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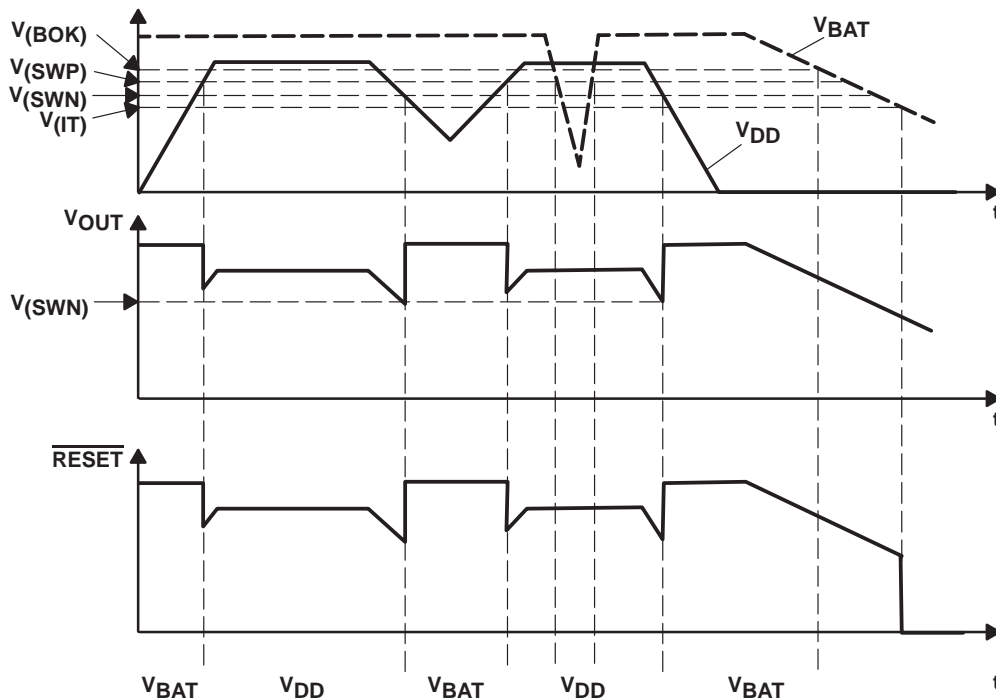
## functional schematic



# TPS3606-33 BATTERY-BACKUP SUPERVISOR FOR LOW-POWER PROCESSORS

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## timing diagram



NOTES: A. MSWITCH = 0,  $\overline{\text{MR}} = 1$

## Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
GND	3	I	Ground
$\overline{\text{MR}}$	7	I	Manual reset input
MSWITCH	4	I	Manual switch to force device into battery-backup mode
PFI	5	I	Power-fail comparator input
$\overline{\text{PFO}}$	6	O	Power-fail comparator output
$\overline{\text{RESET}}$	9	O	Active-low reset output
V(BAT)	10	I	Backup-battery input
V(DD)	2	I	Input supply voltage
V(OUT)	1	O	Supply output
WDI	8	I	Watchdog timer input

**detailed description**

**battery freshness seal**

The battery freshness seal of the TPS3606 family disconnects the backup battery from the internal circuitry until it is needed. This ensures that the backup battery connected to  $V_{BAT}$  is fresh when the final product is put to use. The following steps explain how to enable the freshness seal mode:

1. Connect  $V_{BAT}$  ( $V_{BAT} > V_{BAT(min)}$ )
2. Ground  $\overline{PFO}$
3. Connect PFI to  $V_{DD}$  or  $PFI > V_{(PFI)}$
4. Connect  $V_{DD}$  to power supply ( $V_{DD} > V_{IT}$ )
5. Ground  $\overline{MR}$
6. Power down  $V_{DD}$
7. The freshness seal mode is entered and pins  $\overline{PFO}$  and  $\overline{MR}$  can be disconnected.

The battery freshness seal mode is disabled by the positive-going edge of  $\overline{RESET}$  when  $V_{DD}$  is applied.

**power-fail comparator (PFI and  $\overline{PFO}$ )**

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The power-fail input (PFI) is compared with an internal voltage reference of 1.15 V. If the input voltage falls below the power-fail threshold ( $V_{(PFI)}$ ) of 1.15 V typical, the power-fail output ( $\overline{PFO}$ ) goes low. If it goes above  $V_{(PFI)}$  plus about 12-mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltages above  $V_{(PFI)}$ . The sum of both resistors should be about 1 M $\Omega$ , to minimize power consumption and also to ensure that the current in the PFI pin can be neglected compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of sensed voltage.

If the power-fail comparator is unused, connect PFI to ground and leave  $\overline{PFO}$  unconnected.

**backup-battery switchover**

In the event of a brownout or power failure, it may be necessary to keep a processor running. If a backup battery is installed at  $V_{BAT}$ , the devices automatically connect the processor to backup power when  $V_{DD}$  fails. In order to allow the backup battery (e.g., a 3.6-V lithium cell) to have a higher voltage than  $V_{DD}$ , this family of supervisors does not connect  $V_{BAT}$  to  $V_{OUT}$  when  $V_{BAT}$  is greater than  $V_{DD}$ .  $V_{BAT}$  only connects to  $V_{OUT}$  (through a 2- $\Omega$  switch) when  $V_{OUT}$  falls below  $V_{(SWN)}$  and  $V_{BAT}$  is greater than  $V_{DD}$ . When  $V_{DD}$  recovers, switchover is deferred either until  $V_{DD}$  crosses  $V_{BAT}$ , or when  $V_{DD}$  rises above the threshold ( $V_{(SWP)}$ ).

$V_{DD} > V_{BAT}$	$V_{DD} > V_{(SWN)}$	$V_{OUT}$
1	1	$V_{DD}$
1	0	$V_{DD}$
0	1	$V_{DD}$
0	0	$V_{BAT}$

# TPS3606-33 BATTERY-BACKUP SUPERVISOR FOR LOW-POWER PROCESSORS

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## detailed description (continued)

### manual switchover (MSWITCH)

While operating in the normal mode from  $V_{DD}$ , the device can be manually forced to operate in the battery-backup mode by connecting MSWITCH to  $V_{DD}$ . The table below shows the different switchover modes.

	MSWITCH	Status
<b><math>V_{DD}</math> mode</b>	GND	$V_{DD}$ mode
	$V_{DD}$	Switch to battery-backup mode
<b>Battery-backup mode</b>	GND	Battery-backup mode
	$V_{DD}$	Battery-backup mode

If the manual switchover feature is not used, MSWITCH must be connected to ground.

### watchdog

In a microprocessor- or DSP-based system, it is not only important to supervise the supply voltage, it is also important to ensure the correct program execution. The task of a watchdog is to ensure that the program is not stalled in an indefinite loop. The microprocessor, microcontroller, or the DSP has to toggle the watchdog input within typically 0.8 s to avoid a time-out from occurring. Either a low-to-high or a high-to-low transition resets the internal watchdog timer. If the input is unconnected, the watchdog is disabled and is retriggered internally.

### saving current while using the watchdog

The watchdog input is internally driven low during the first 7/8 of the watchdog time-out period, then momentarily pulses high, resetting the watchdog counter. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog time-out period, pulsing it low-high-low once within 7/8 of the watchdog time-out period to reset the watchdog timer. If instead, WDI is externally driven high for the majority of the time-out period, a current of e.g.  $5\text{ V}/40\text{ k}\Omega \approx 125\ \mu\text{A}$  can flow into WDI.

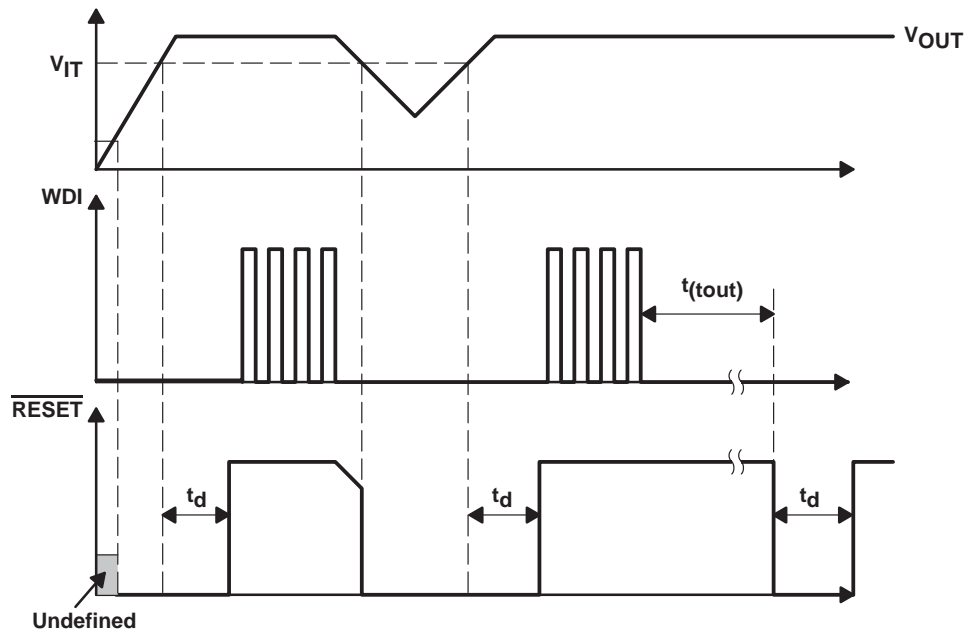


Figure 1. Watchdog Timing

# TPS3606-33

## BATTERY-BACKUP SUPERVISOR FOR LOW-POWER PROCESSORS

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### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage: $V_{DD}$ (see Note1) .....	7 V
$\overline{MR}$ , WDI, and PFI pins (see Note 1) .....	–0.3 V to ( $V_{DD} + 0.3$ V)
Continuous output current at $V_{OUT}$ : $I_O$ .....	300 mA
All other pins, $I_O$ .....	±10 mA
Continuous total power dissipation .....	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ .....	–40°C to 85°C
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds .....	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than  $t = 1000h$  continuously.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DGS	424 mW	3.4 mW/°C	271 mW	220 mW

### recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, $V_{DD}$	1.65	5.5	V
Battery supply voltage, $V_{BAT}$	1.5	5.5	V
Input voltage, $V_I$	0	$V_O + 0.3$	V
High-level input voltage, $V_{IH}$	$0.7 \times V_O$		V
Low-level input voltage, all other pins, $V_{IL}$		$0.3 \times V_O$	V
Continuous output current at $V_{OUT}$ : $I_O$		200	mA
Input transition rise and fall rate at WDI, MSWITCH, $\Delta t/\Delta V$		100	ns/V
Slew rate at $V_{DD}$ or $V_{BAT}$		34	mV/ $\mu\text{s}$
Operating free-air temperature range, $T_A$	–40	85	°C

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## BATTERY-BACKUP SUPERVISOR FOR LOW-POWER PROCESSORS

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### electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	$\overline{\text{RESET}}$ V <sub>OUT</sub> = 2 V, I <sub>OH</sub> = -400 μA	V <sub>OUT</sub> - 0.2 V			V
			V <sub>OUT</sub> = 3.3 V, I <sub>OH</sub> = -2 mA V <sub>OUT</sub> = 5 V, I <sub>OH</sub> = -3 mA	V <sub>OUT</sub> - 0.4 V		
		$\overline{\text{PFO}}$ V <sub>OUT</sub> = 1.8 V, I <sub>OH</sub> = -20 μA	V <sub>OUT</sub> - 0.3 V			
			V <sub>OUT</sub> = 3.3 V, I <sub>OH</sub> = -80 μA V <sub>OUT</sub> = 5 V, I <sub>OH</sub> = -120 μA	V <sub>OUT</sub> - 0.4 V		
V <sub>OL</sub>	Low-level output voltage	$\overline{\text{RESET}}$ V <sub>OUT</sub> = 2 V, I <sub>OL</sub> = 400 μA	0.2			V
		$\overline{\text{PFO}}$ V <sub>OUT</sub> = 3.3 V, I <sub>OL</sub> = 2 mA V <sub>OUT</sub> = 5 V, I <sub>OL</sub> = 3 mA	0.4			
		V <sub>res</sub>	Power-up reset voltage (see Note 2)			
V <sub>OUT</sub>	Normal mode	I <sub>O</sub> = 5 mA, V <sub>DD</sub> = 1.8 V	V <sub>DD</sub> - 50 mV			V
		I <sub>O</sub> = 75 mA, V <sub>DD</sub> = 3.3 V	V <sub>DD</sub> - 150 mV			
		I <sub>O</sub> = 150 mA, V <sub>DD</sub> = 5 V	V <sub>DD</sub> - 250 mV			
	Battery-backup mode	I <sub>O</sub> = 4 mA, V <sub>BAT</sub> = 1.5 V	V <sub>BAT</sub> - 50 mV			
		I <sub>O</sub> = 75 mA, V <sub>BAT</sub> = 3.3 V	V <sub>BAT</sub> - 150 mV			
r <sub>ds(on)</sub>	V <sub>DD</sub> to V <sub>OUT</sub> on-resistance	V <sub>DD</sub> = 3.3 V	1		2	Ω
	V <sub>BAT</sub> to V <sub>OUT</sub> on-resistance	V <sub>BAT</sub> = 3.3 V	1		2	
V <sub>IT</sub>	Negative-going input threshold voltage (see Notes 3 and 4)	TPS3606x33	2.87	2.93	2.99	V
V <sub>(PFI)</sub>	Power-fail input threshold voltage	PFI	1.13	1.15	1.17	
V <sub>(SWN)</sub>	Battery switch threshold voltage negative-going V <sub>OUT</sub>		V <sub>IT</sub> + 1%	V <sub>IT</sub> + 2%	V <sub>IT</sub> + 3.2%	V

- NOTES:
- The lowest supply voltage at which  $\overline{\text{RESET}}$  becomes active.  $t_r(\text{VDD}) \geq 15 \mu\text{s/V}$ .
  - To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed near the supply terminal.
  - Voltage is sensed at V<sub>OUT</sub>
  - For details on how to optimize current consumption when using WDI refer to section detailed description.



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electrical characteristics over recommended operating conditions (unless otherwise noted)  
(continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{hys}$	Hysteresis	$V_{IT}$	$1.65\text{ V} < V_{IT} < 2.5\text{ V}$		20	mV	
			$2.5\text{ V} < V_{IT} < 3.5\text{ V}$		40		
			$3.5\text{ V} < V_{IT} < 5.5\text{ V}$		50		
	$V_{PFI}$			12			
	$V_{(SWN)}$	$1.65\text{ V} < V_{(SWN)} < 2.5\text{ V}$		85			
		$2.5\text{ V} < V_{(SWN)} < 3.5\text{ V}$		100			
$3.5\text{ V} < V_{(SWN)} < 5.5\text{ V}$		110					
$I_{IH}$	High-level input current	$\overline{WDI}$	$\overline{WDI} = V_{DD} = 5.5\text{ V}$		150	$\mu\text{A}$	
		$\overline{MR}$	$\overline{MR} = 0.7 \times V_{DD}, V_{DD} = 5\text{ V}$		-33	-76	
$I_{IL}$	Low-level input current	$\overline{WDI}$	$\overline{WDI} = 0\text{ V}, V_{DD} = 5\text{ V}$		-150		
		$\overline{MR}$	$\overline{MR} = 0\text{ V}, V_{DD} = 5\text{ V}$		-110	-255	
$I_I$	Input current	PFI, MSWITCH	$V_I < V_{DD}$		-25	25	nA
$I_{OS}$	Short-circuit current	$\overline{PFO}$	$\overline{PFO} = 0\text{ V}, V_{DD} = 1.8\text{ V}$		-0.3	mA	
			$\overline{PFO} = 0\text{ V}, V_{DD} = 3.3\text{ V}$		-1.1		
			$\overline{PFO} = 0\text{ V}, V_{DD} = 5\text{ V}$		-2.4		
$I_{DD}$	$V_{DD}$ supply current	$V_{OUT} = V_{DD}$		40		$\mu\text{A}$	
		$V_{OUT} = V_{BAT}$		8			
$I_{(BAT)}$	$V_{BAT}$ supply current	$V_{OUT} = V_{DD}$		-0.1	0.1	$\mu\text{A}$	
		$V_{OUT} = V_{BAT}$		40			
$C_i$	Input capacitance	$V_I = 0\text{ V to } 5\text{ V}$		5		pF	

timing requirements at  $R_L = 1\text{ M}\Omega$ ,  $C_L = 50\text{ pF}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_w$	Pulse width	$V_{DD}$	$V_{IH} = V_{IT} + 0.2\text{ V}, V_{IL} = V_{IT} - 0.2\text{ V}$		5	$\mu\text{s}$
		$\overline{MR}$	$V_{DD} > V_{IT} + 0.2\text{ V}, V_{IL} = 0.3 \times V_{DD}, V_{IH} = 0.7 \times V_{DD}$		100	
		$\overline{WDI}$				

switching characteristics at  $R_L = 1\text{ M}\Omega$ ,  $C_L = 50\text{ pF}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$t_d$	Delay time	$V_{DD} \geq V_{IT} + 0.2\text{ V}, \overline{MR} \geq 0.7 \times V_{DD}$ . See timing diagram	60	100	140	ms	
$t_{(tout)}$	Watchdog time-out	$V_{DD} > V_{IT} + 0.2\text{ V}$ , See timing diagram	0.48	0.8	1.12	s	
$t_{PHL}$	Propagation (delay) time, high-to-low-level output	$V_{DD}$ to $\overline{\text{RESET}}$	$V_{IL} = V_{IT} - 0.2\text{ V}, V_{IH} = V_{IT} + 0.2\text{ V}$		2	5	$\mu\text{s}$
		PFI to $\overline{PFO}$	$V_{IL} = V(\text{PFI}) - 0.2\text{ V}, V_{IH} = V(\text{PFI}) + 0.2\text{ V}$		3		$\mu\text{s}$
		$\overline{MR}$ to $\overline{\text{RESET}}$	$V_{DD} \geq V_{IT} + 0.2\text{ V}, V_{IL} = 0.3 \times V_{DD}, V_{IH} = 0.7 \times V_{DD}$		0.1	1	$\mu\text{s}$
Transition time		$V_{DD}$ to $V_{BAT}$	$V_{IL} = V(\text{BAT}) - 0.2\text{ V}, V_{IH} = V(\text{BAT}) + 0.2\text{ V}, V(\text{BAT}) < V_{IT}$		3		$\mu\text{s}$

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## TYPICAL CHARACTERISTICS

### Table of Graphs

			FIGURE
$r_{DS(on)}$	Static drain-source on-state resistance ( $V_{DD}$ to $V_{OUT}$ )	vs Output current	2
	Static drain-source on-state resistance ( $V_{BAT}$ to $V_{OUT}$ )	vs Output current	3
$I_{DD}$	Supply current	vs Supply voltage	4
		vs Battery supply	5
$V_{IT}$	Input threshold voltage at $\overline{RESET}$	vs Free-air temperature	6
$V_{OH}$	High-level output voltage at $\overline{RESET}$	vs High-level output current	7, 8
	High-level output voltage at $\overline{PFO}$		9, 10
$V_{OL}$	Low-level output voltage at $\overline{RESET}$	vs Low-level output current	11, 12
	Minimum pulse duration at $V_{DD}$	vs Threshold voltage overdrive at $V_{DD}$	13
	Minimum pulse duration at $PFI$	vs Threshold voltage overdrive at $PFI$	14

**STATIC DRAIN SOURCE ON-STATE RESISTANCE  
( $V_{DD}$  TO  $V_{OUT}$ )  
vs  
OUTPUT CURRENT**

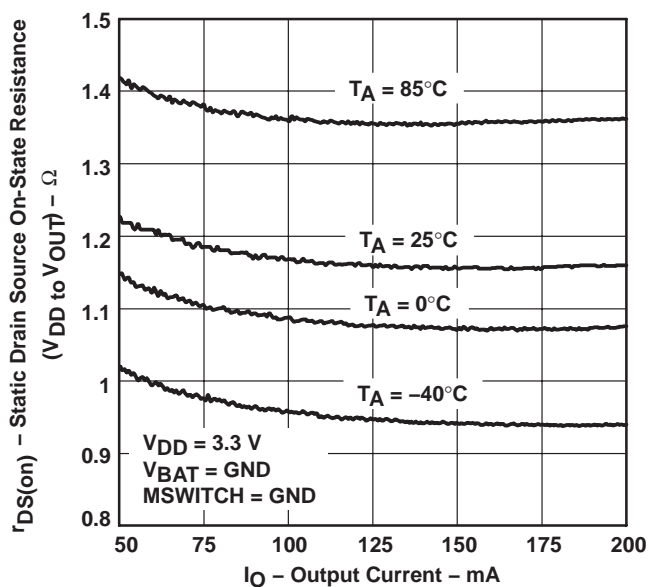


Figure 2

**STATIC DRAIN SOURCE ON-STATE RESISTANCE  
( $V_{BAT}$  TO  $V_{OUT}$ )  
vs  
OUTPUT CURRENT**

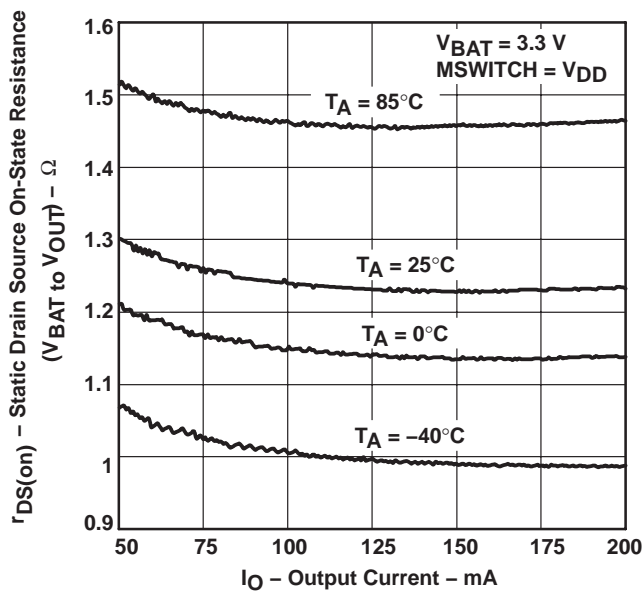
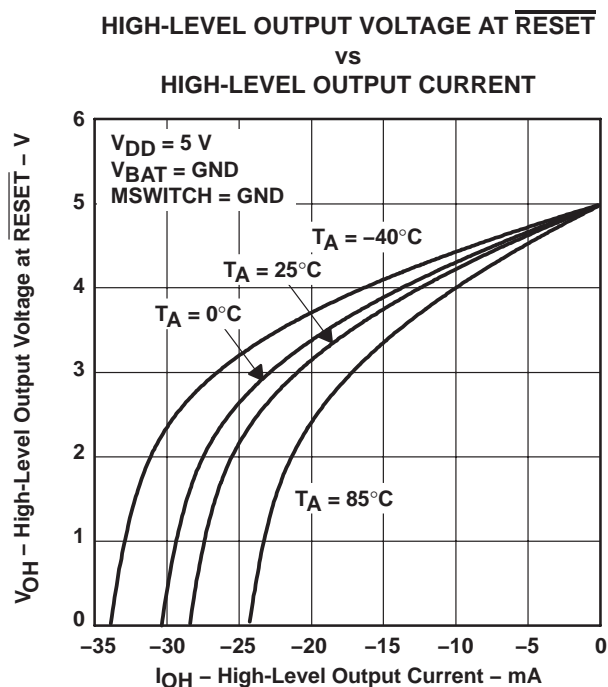
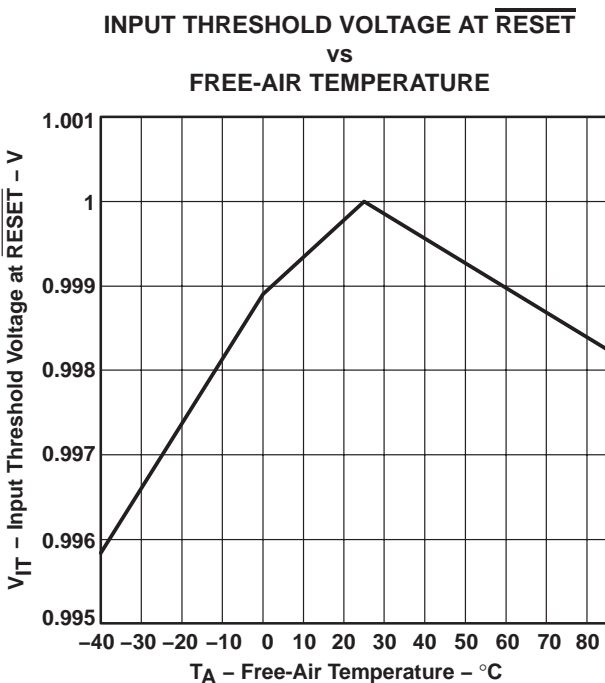
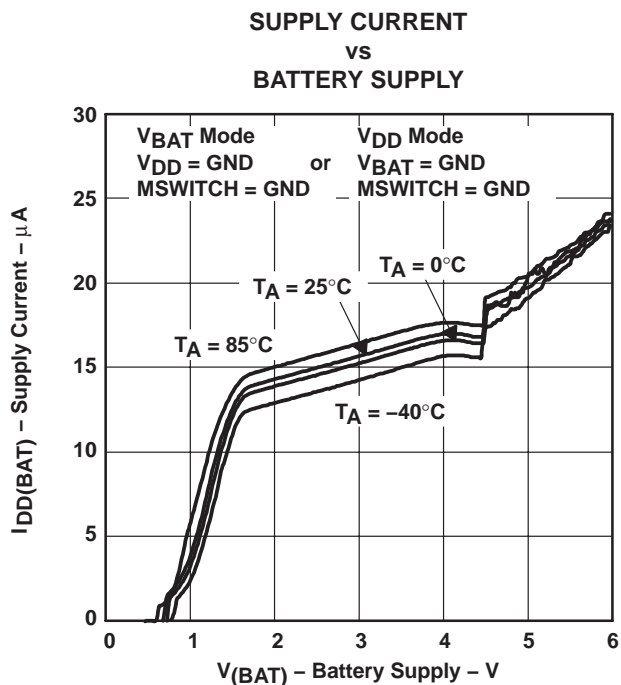
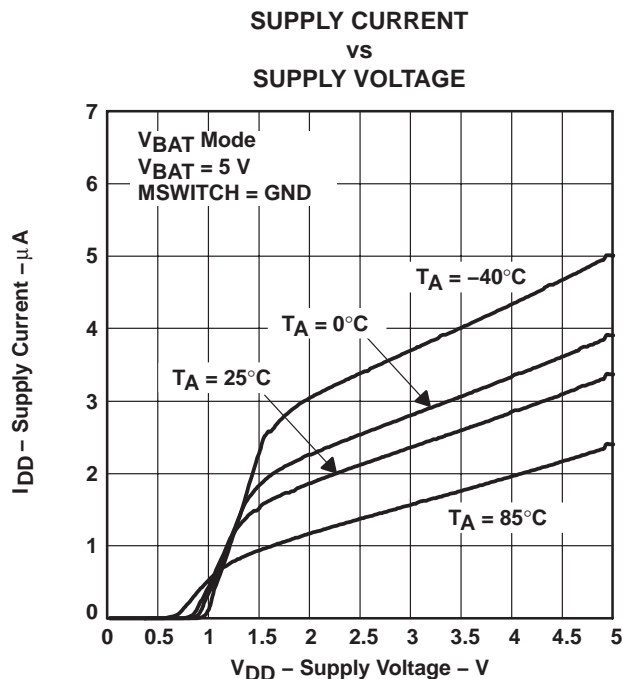


Figure 3

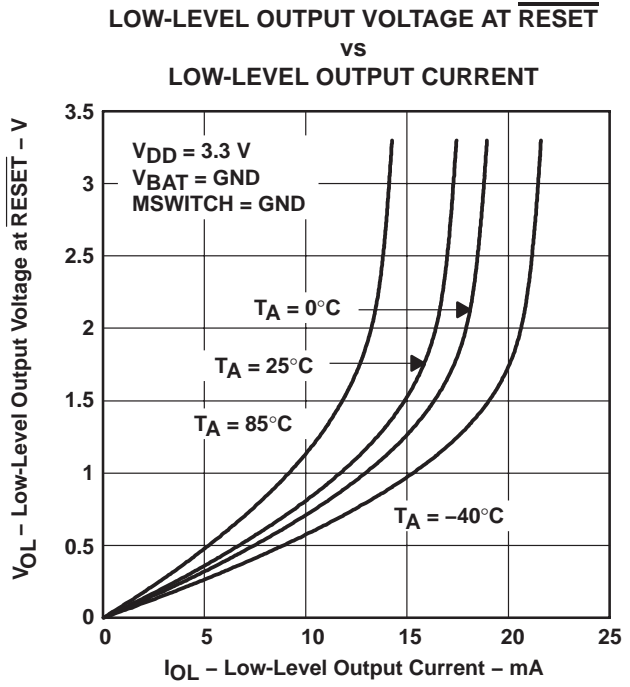
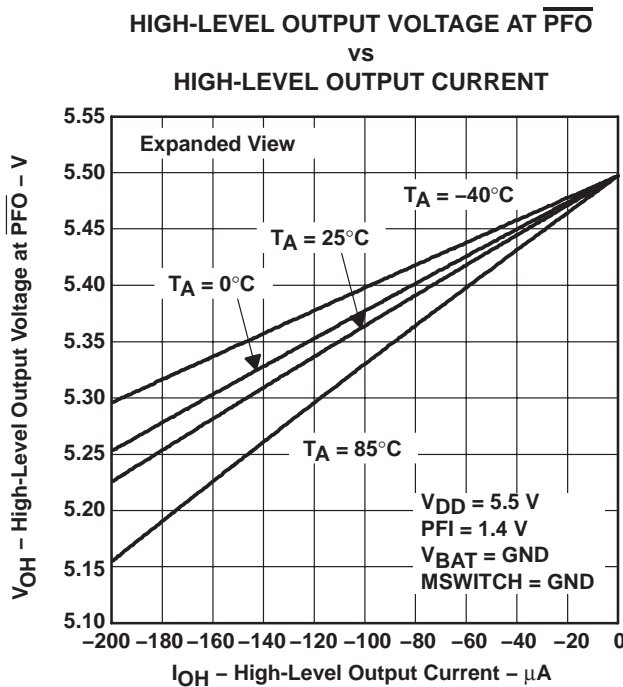
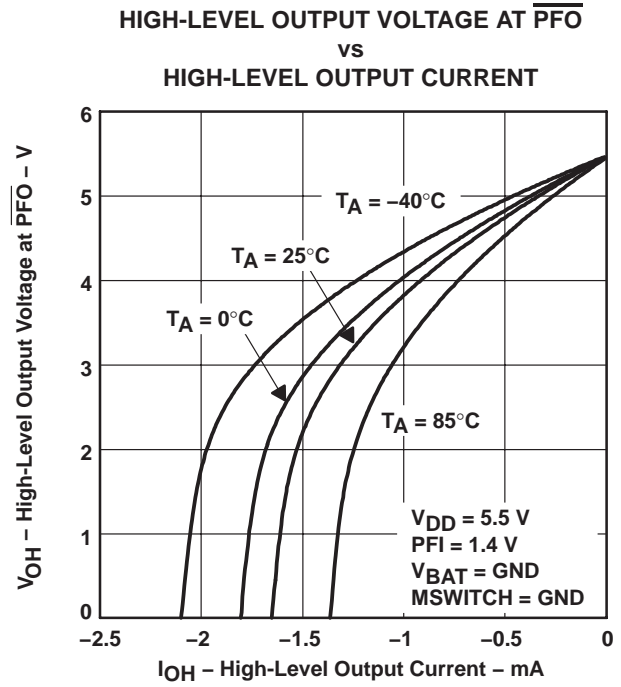
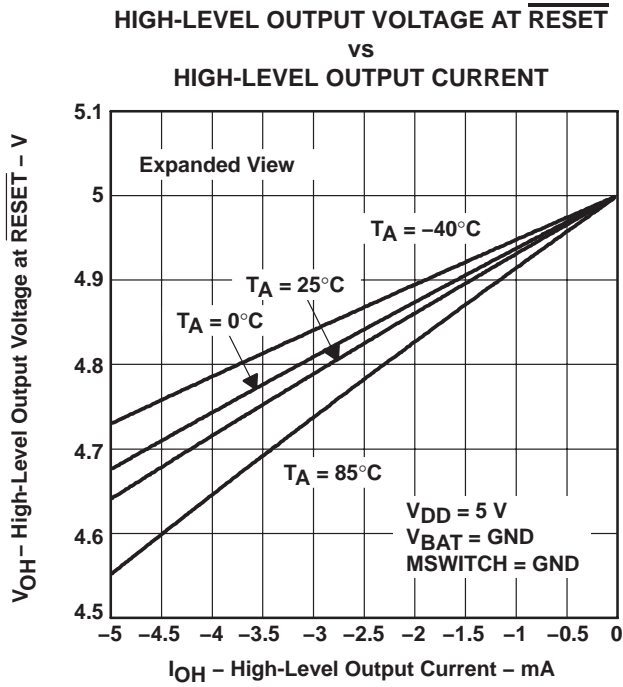
**TYPICAL CHARACTERISTICS**



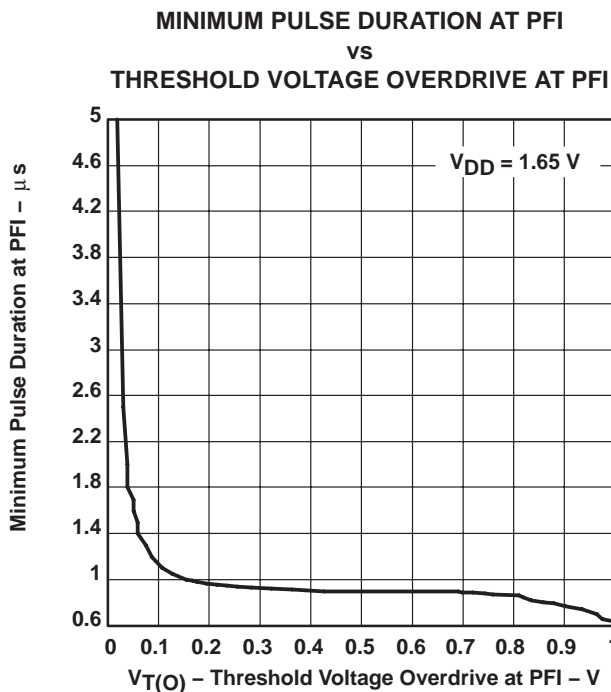
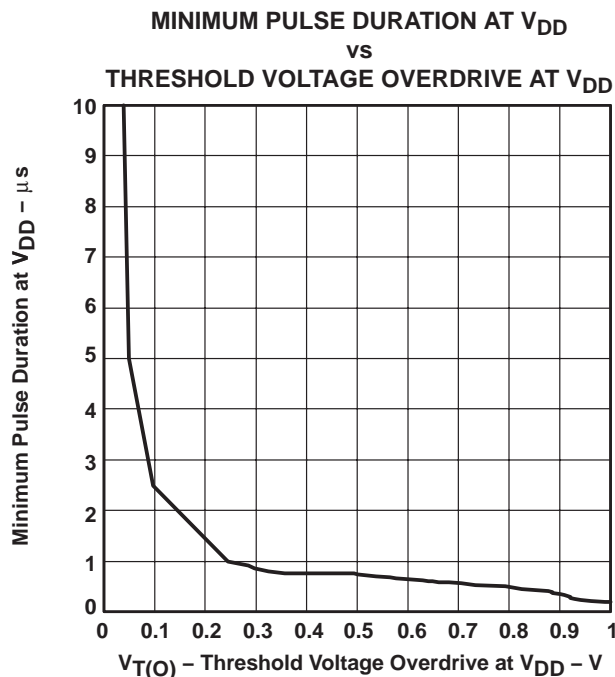
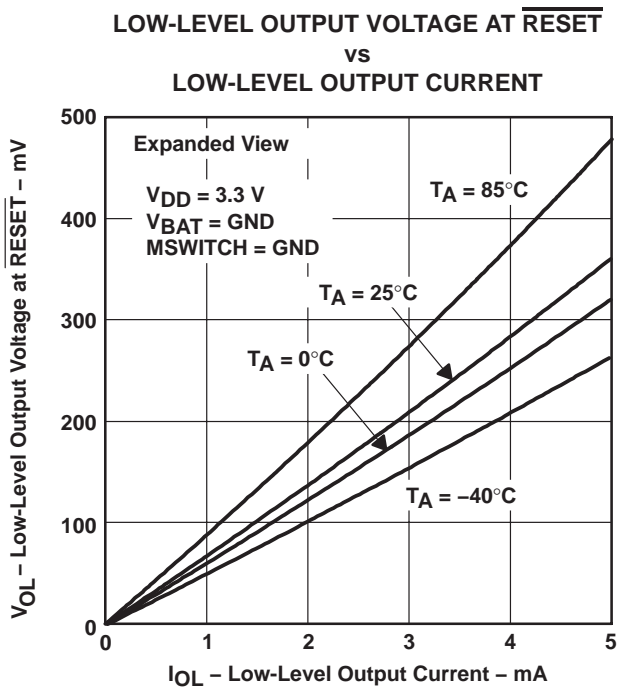
# TPS3606-33 BATTERY-BACKUP SUPERVISOR FOR LOW-POWER PROCESSORS

SLVS335C – DECEMBER 2000 – REVISED JANUARY 2007

## TYPICAL CHARACTERISTICS



**TYPICAL CHARACTERISTICS**



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS3606-33DGS	ACTIVE	MSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3606-33DGSG4	ACTIVE	MSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3606-33DGSR	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3606-33DGSRG4	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3606-33DGSR	MSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3606-33DGSR	MSOP	DGS	10	2500	358.0	335.0	35.0



DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Falls within JEDEC MO-187 variation BA.

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